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(54) Memory board stacking module

(57) A memory board stacking module comprises a mother board (10) having female input/output sockets (12) in electrical connection with mother board circuitry. A first memory board (20) carrying memory chips (22) is connected by an input/output conductor scheme to a first row (28) of input/output stacking contacts (32*a*) each of the stacking contacts having a female socket end (34*a*) supported in the first memory board and a male end (36*a*) opposite thereto, each male end being removably received in one of the female sockets (12) of the mother board. A second memory board (40) carrying memory chips (22) is connected by an input/output conductor scheme to a first row (48) of input/output stacking contacts (32*b*), each of the stacking contacts having a female socket end (34*b*) supported in the second memory board and a male end (36*b*) opposite thereto, each of the male ends (36*b*) of the stacking contacts of the said second memory board (40) being removably received in one of the female socket ends (34*a*) of the stacking contact of the first memory board (20). The stacking contacts electrically connect the memory chips of the first memory board and the memory chips of the second memory board with the mother board circuitry.

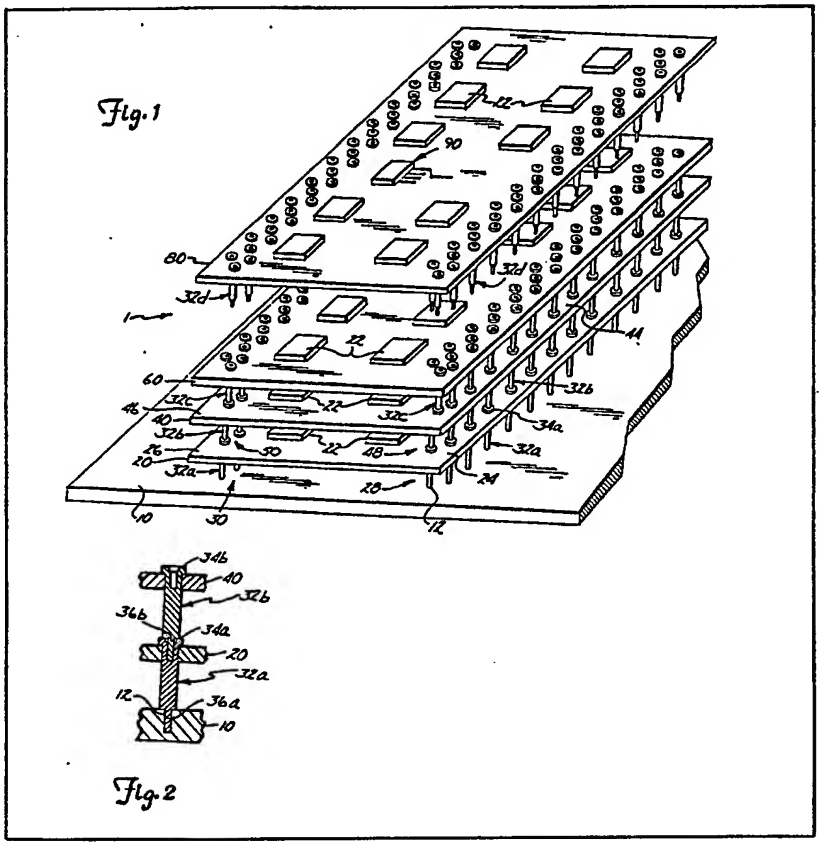

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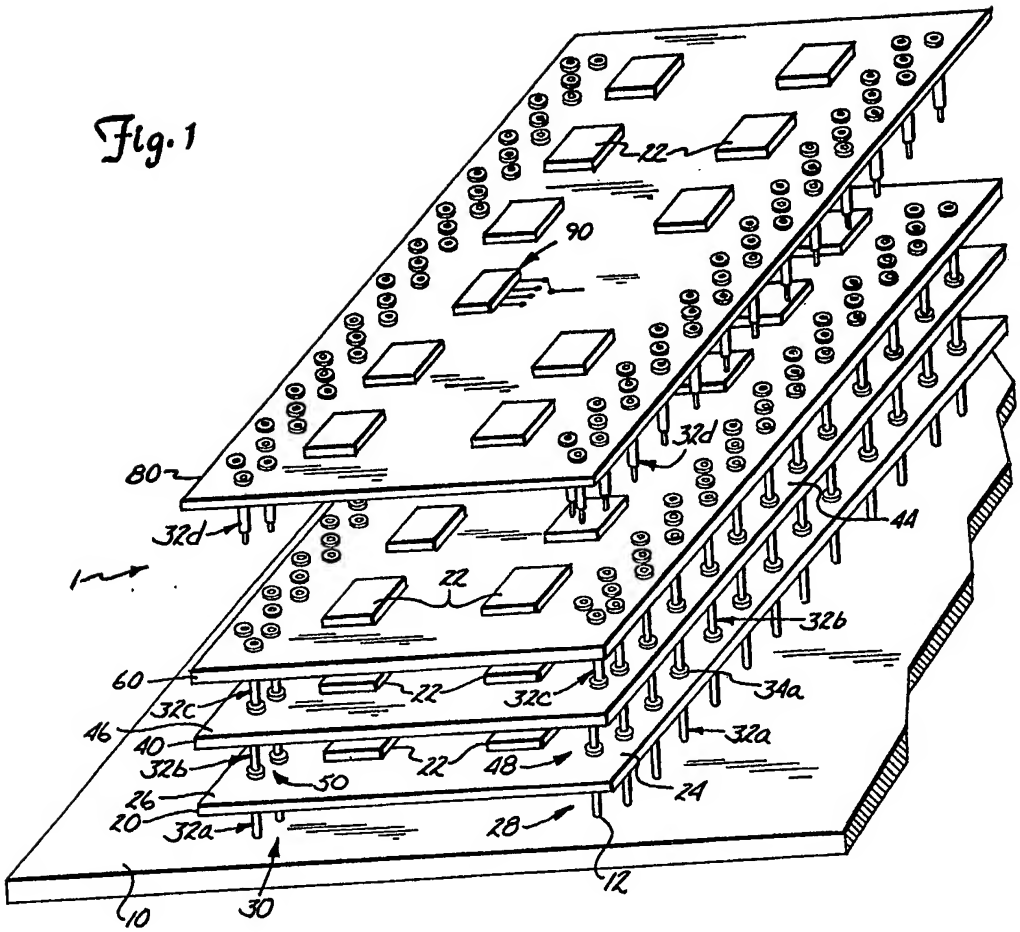
Fig. 1



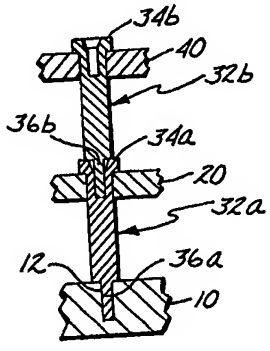
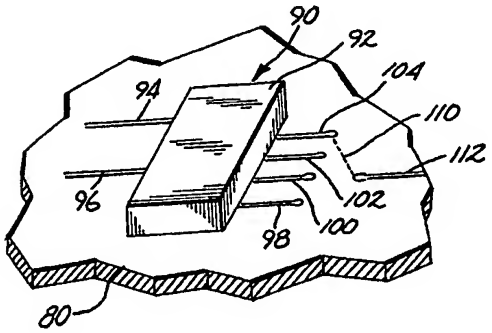


Fig. 2

Fig. 3



SPECIFICATION

Memory board stacking module

This invention relates to memory board stacking modules.

Prior stacking modules of memory boards cannot be tailored to fit the special needs of the user and easily expanded as necessary to fit the changing needs of the user.

Although the present invention is primarily directed to any novel integer or step, or combination of integers or steps, herein disclosed and/or as shown in the accompanying drawings, nevertheless, according to one particular aspect of the present invention to which, however, the invention is in no way restricted, there is provided a memory board stacking module comprising: a mother board having a plurality of female input/output sockets in electrical connection with mother board circuitry; a first memory board carrying memory chips connected by an input/output conductor scheme to a first row of input/output stacking contacts, each of said stacking contacts having a female socket end supported in said first memory board and a male end opposite thereto, each of said male ends of said stacking contacts being removably received in one of said female sockets of said mother board; and a second memory board carrying memory chips connected by an input/output conductor scheme to a first row of input/output stacking contacts, each of said stacking contacts having a female socket end supported in said second memory board and a male end opposite thereto, each of said male ends of said stacking contacts of said second memory board being removably received in one of said female socket ends of said stacking contacts of said first memory board, said stacking contacts electrically connecting said memory chips of said first memory board and said memory chips of said second memory board with said mother board circuitry.

Preferably said first memory board is rectangular and has a first edge region and a second edge region opposite thereto, said first row of stacking contacts being disposed along said first edge region, a second row of stacking contacts being disposed along said second edge region, said second row of stacking contacts being electrically connected by means of said input/output conductor scheme with said memory chips of said first memory board, said second memory board being rectangular and having a first edge region and a second edge region opposite thereto, said first row of stacking contacts being disposed along said first edge region of said second memory board, a second row of stacking contacts being disposed along said second edge region of said second memory board, said second row of stacking contacts being electrically connected by said input/output conductor scheme to said memory chips of said second memory board, each of said male ends of said second row of stacking contacts of said second memory board being removably received in one of said female socket ends of said first memory board.

Said first memory board and said second memory board may have substantially identical input/output conductor schemes connecting said memory chips to said stacking contacts.

Said first memory board and said second memory board preferably are substantially identical.

The module may include means on said first and second memory boards for selectively inputting data thereto. Thus said first and second memory boards may be identical except for said means.

In the preferred embodiment the module includes a third memory board secured to said second memory board in a piggy-back configuration, said third memory board having a row of stacking contacts, male ends of which are removably received in said female socket ends of said stacking contacts of said second memory board, said third memory board being substantially identical to said first and second memory boards.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:—

Figure 1 is a partially-exploded perspective view of a memory board stacking module according to the present invention;

Figure 2 is a cross-sectional view showing stacking contacts of the module of Figure 1; and

Figure 3 is a perspective view of board selection circuitry of the module of Figure 1.

A memory board stacking module 1 according to the present invention and as shown in Figure 1 is composed of a mother board 10, a first memory board 20, a second memory board 40, a third memory board 60, and a fourth memory board 80 arranged in a piggy-back configuration.

The boards 20, 40, 60, 80 are substantially identical and the board 20 will be described first. The board 20 carries a plurality of memory chips 22 and is rectangular in shape having a first edge region 24 and an opposite edge region 26. The first edge region 24 includes one or more rows 28 of stacking contacts 32*a* and the second edge region 26 includes one or more rows 30 of stacking contact 32*a*.

The stacking contacts 32*a* are best shown in Figure 2. Each stacking contact 32*a* has a female socket end 34*a* secured in the board 20 and a male end 36*a* opposite thereto. Each of the male ends 36*a* is removably secured in a suitable input/output plated aperture or female socket 12 of the mother board 10. The socket ends 34*a* are electrically connected by means of an input/output conductor scheme (not shown) to pins (not shown) of the memory chips 22, either directly or through other circuitry on the board. This input/output conductor scheme is identical for each board. Hence, the contacts 32*a* comprise input/output pins which electrically interconnect the memory chips 22 of the board 20 with the circuitry (not shown) of the mother board 10.

The board 40 which is substantially identical to the board 20, is stacked or piggy-backed on top of the latter to expand the memory capacity of the module 1. The board 40, being substantially identical to the board 20, carries identically arranged memory chips 22 which are connected by an identical input/output scheme (not shown) to stacking contacts 32*b*. The board 40 has a first edge region 44 and a second edge region 46 opposite thereto. One or more rows 48 of the stacking contacts 32*b* are disposed along the edge region 44. Likewise one or more rows 50 of the stacking contacts 32*b* are disposed along the edge region 46. Referring again to Figure 2, each of the stacking contacts 32*b* has a female socket end 34*b* secured in the board 40 and a male end 36*b* opposite thereto. Each of the male ends 36*b* is removably secured in a female socket end 34*a* of a corresponding stacking contact 32*a* of the board 20. In that the memory chips 22 of the board 40 are electrically interconnected to the stacking contacts 32*b* by an input/output circuit scheme identical to that for the board 20, and in that each of the stacking contacts 32*b* is electrically interconnected to a corresponding stacking contact 32*a* of the board 20, the memory chips 22 of the board 40 are electrically interconnected with the circuitry of the mother board 40 through the contacts 32*a*, 32*b*.

The board 60 is substantially identical to the boards 20, 40 and is piggy-backed on the board 40 by stacking contacts 32*c* in the same manner as described above. Likewise, the board 80 is piggy-backed to the board 60 by means of stacking contacts 32*d*.

It has been stated that the boards 20, 40, 60, 80 are "substantially identical" in that they have an identical arrangement of the memory chips 22, and an identical input/output conductor scheme connecting the memory chips 22 to the stacking contacts 32*a* to 32*b* respectively. Moreover, the stacking contacts 32*a* to 32*b* are all arranged in identical patterns on the boards 20, 40, 60, 80 so that they can be stacked. Given this identity of construction between the boards 20, 40, 60, 80, they are nevertheless referred to as "substantially identical" in that each of the boards 20, 40, 60, 80, includes slightly different board selection circuitry to allow the incoming data to be fed only into the one board to which it is intended.

Figure 3 shows board selection circuitry 90 which is installed on each of the boards 20, 40, 60, 80. The circuitry 90 comprises an industry standard 74F, 139, TTL 2—4 Decoder, chip 92, having two inputs 94, 96, and four outputs 98, 100, 102, 104. Each group of data which is input to the module 1 includes two digital board selection data bits. Each of these two bits travel up a designated column of the stacking contacts 32*a* to 32*d* and is fed to the chip 92 on each board. The chips 92 then decode the signals fed to their inputs 94, 96 to determine which of the outputs 98, 100, 102, 104 will be enabled. For example, if we use "0" to indicate a low signal, and "1" to represent a high signal, an input of 0,0 would enable output 98; 0,1 would enable output 100; 1,0 would enable output 102; 1,1 would enable output 104. On each of the boards 20, 40, 60, 80, only one of the outputs 98, 100, 102, 104 will be electrically connected to the input/output conductor scheme, with the remaining outputs being open circuited. Thus, on the board 20, only the output 98 is electrically connected and outputs 100, 102, 104 are open; on the board 40 only the output 100 is connected, and outputs 98, 102, 104 are open; on the board 60 only the output 102 is connected and outputs 98, 100, 104 are open; and on the board 80 only the output 104 is connected and outputs 98, 100, 102 are open. Figure 3 indicates by a dotted line 110 the electrical connection for the board 80 comprising a jumper connected from the output 104 to an input/output conductor scheme 112 of the board 80.

Consequently, if a group of data is intended to be fed into the memory chips 22 of the board 80, the two board selection data bits fed through the inputs 94, 96 will be 1,1. In response to the input 1,1, the chip 92 on each board will enable the output 104. However, since the output 104 is open circuited on boards 20, 40, 60, and electrically connected only on the board 80, the data will be fed to the memory chips of the board 80 only. Thus, as groups of data are fed into the module 1, through the columns of stacking contacts 32*a* to 32*d*, the data arrives at each of the boards 20, 40, 60, 80, but is input into the memory chips 22 of one of the boards only as determined by the two board selection data bits.

Having disclosed the basic structure of one embodiment of the present invention, its advantages can be appreciated. First, the boards 20, 40, 60, 80, being identical as to the arrangement of memory chips each have the same memory capacity. Hence, each board 20, 40, 60, 80, can be thought of as a memory unit. Moreover, the boards are removably secured to one another. Therefore, in order to expand or vary the memory capacity of the module 1, the boards can either be added to or removed from the module. This feature is especially advantageous in that the capacity of the modules can be tailored to the needs of a user and can be expanded as the needs of the user change, with minimal effort and expense. Furthermore, should one of the boards 20, 40, 60, 80, become defective, it can be easily removed and replaced by an identical board with a jumper connected from the conductor scheme to the appropriate output 98, 100, 102, 104.

CLAIMS

1. A memory board stacking module comprising: a mother board having a plurality of female input/output sockets in electrical connection with mother board circuitry; a first memory board carrying memory chips connected by an input/output conductor scheme to a first row of input/output stacking contacts, each of said stacking contacts having a female socket end supported in said first memory board and a male

end opposite thereto, each of said male ends of said stacking contacts being removably received in one of said female sockets of said mother board; and a second memory board carrying memory chips connected by an input/output conductor scheme to a first row of input/output stacking contacts, each of said stacking contacts having a female socket end supported in said second memory board and a male end opposite thereto, each of said male ends of said stacking contacts of said second memory board being removably received in one of said female socket ends of said stacking contacts of said first memory board, said stacking contacts electrically connecting said memory chips of said first memory board and said memory chips of said second memory board with said mother board circuitry.

2. A module as claimed in claim 1 in which said first memory board is rectangular and has a first edge region and a second edge region opposite thereto, said first row of stacking contacts being disposed along said first edge region, a second row of stacking contacts being disposed along said second edge region, said second row of stacking contacts being electrically connected by means of said input/output conductor scheme with said memory chips of said first memory board, said second memory board being rectangular and having a first edge region and a second edge region opposite thereto, said first row of stacking contacts being disposed along said first edge region of said second memory board, a second row of stacking contacts being disposed along said second edge region of said second memory board, said second row of stacking contacts being electrically connected by said input/output conductor scheme to said memory chips of said second memory board, each of said male ends of said second row of stacking contacts of said second memory board being removably received in one of said female socket ends of said second row of stacking contacts of said first memory board.

3. A module as claimed in claim 1 or 2 in which said first memory board and said second memory board have substantially identical input/output conductor schemes connecting said memory chips to said stacking contacts.

4. A module as claimed in any preceding claim in which said first memory board and said second memory board are substantially identical.

5. A module as claimed in any preceding claim including means on said first and second memory boards for selectively inputting data thereto.

6. A module as claimed in claim 5 in which said first and second memory boards are identical except for said means.

7. A module as claimed in any preceding claim including a third memory board secured to said second memory board in a piggy-back configuration, said third memory board having a row of stacking contacts, male ends of which are removably received in said female socket ends of said stacking contacts of said second memory board, said third memory board being substantially identical to said first and second memory boards.

8. A memory board stacking module substantially as herein described with reference to and as shown in the accompanying drawings.

9. Any novel integer or step, or combination of integers or steps, hereinbefore described, irrespective of whether the present claim is within the scope of, or relates to the same or a different invention from that of, the preceding claims.

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